

A Completely Integrated 1.8 Volt 5GHz Tunable Image Reject Notch Filter

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Abstract — This paper presents a topology for an integrated image reject notch filter. The filter circuitry is combined with a standard LNA topology thus minimizing the additional current required to perform this function on-chip. In applications where NF is not the dominant consideration, the filter could do double duty as an LNA stage. A prototype circuit exhibited the following performance: 70dB of image rejection, a NF of 4.2dB, 14dB of gain in the pass band, and an IIP3 of -6dBm.

I. INTRODUCTION

Superheterodyne receivers are one of the most common front-end architectures in use today. However they resist efforts to raise integration because they require high quality filters to remove the image before the signal is down converted to an IF frequency. The image filter is required to suppress the unwanted image frequency, which is located two IFs away from the desired radio frequency. Recently, there have been efforts to replace these off-chip filters with on-chip active notch filters [1]-[4]. In this paper, an alternative circuit topology for the filter is presented. This topology reflects the image at the input and never lets it enter the radio. By dealing with the image at an early stage, linearity problems are reduced since the image hasn't been amplified by preceding stages.

II. CIRCUIT DESIGN

The circuit shown in Fig. 1 provides notching action in a conventional LNA topology. Previous circuit topologies have employed an additional stage following the LNA that performed the image rejection. In the approach discussed here, the conventional topology for a cascode LNA shown in Fig. 1 is modified by adding a resonator around inductor L_e . The LC resonator at the emitter of Q1 will be centered at the notch frequency and will present a high impedance to the emitter of the driving transistor. A high impedance at the notch frequency will reduce the driver gain (ideally to zero). In effect, the image will be reflected. Below the resonance frequency of the LC tank, the resonator will look inductive and will have an impedance close to that of the actual inductor placed in the circuit. Thus, in the pass

band, the circuit will perform and operate like an LNA with inductive degeneration.

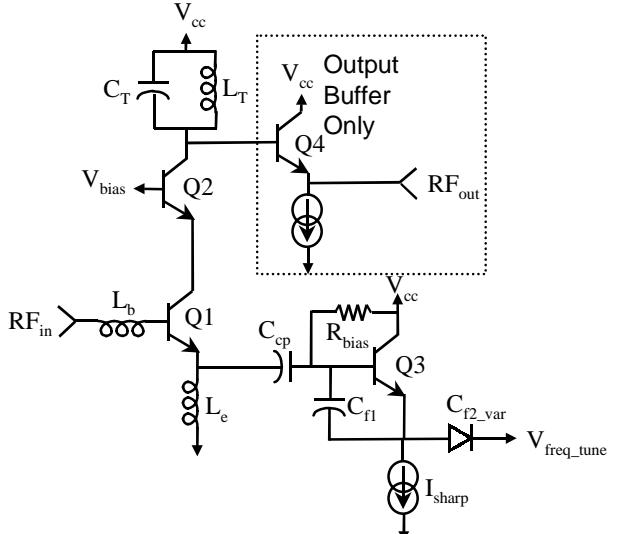


Fig. 1. LNA circuit with resonator placed in the emitter to provide a high impedance at the undesired image frequency.

Unfortunately, there will be losses associated with the LC resonator, which will seriously impact its effectiveness. Thus, some form of active circuitry must be added in addition to a simple capacitor in parallel with the inductor. A simple way to implement this is to add feedback around two series capacitors (C_{f1} and C_{f2_var}) as shown in Fig. 1. Note that one of the capacitors C_{f2_var} must be implemented using a varactor to make the filter tunable. Due to process variations, the current I_{sharp} may need to be tuned as well to ensure perfect cancellation of the losses in the resonator.

In the design of the circuit two inductors (L_b , L_e) are used to provide simultaneous noise and power matching of the circuit in the pass band. The procedure for doing this is described in detail in [5]. The tank formed by L_T and C_T is tuned to the pass band frequency and will provide some additional image rejection for the filter.

For the purposes of measurement, an output buffer was added to drive the measurement equipment in the test circuit. Emitter follower Q4 formed the buffer. In an actual application where the filter would drive a mixer on the same chip, the buffer would be removed.

III. FILTER STABILITY

When dealing with filters and high Q resonators, stability is always a concern. In particular with the circuit topology shown here, beyond the notch frequency there will be a large negative resistance generated looking into the base due to the presence of the capacitance C_E in the resonator. This analysis can also be used to show the operation of the circuit, but equations often generate less insight than a qualitative description of the circuit.

For the purposes of this analysis, the simplified small-signal model for the circuit shown in Fig. 2 will be used. Here the complex resistance is reflected into the base and is placed in series with the transistor's input impedance Z_π . The output is modeled as a simple voltage controlled current source driving the tank at the collector of the cascode transistor. For the purposes of this analysis the cascode is assumed to have a current gain of one with no phase shift.

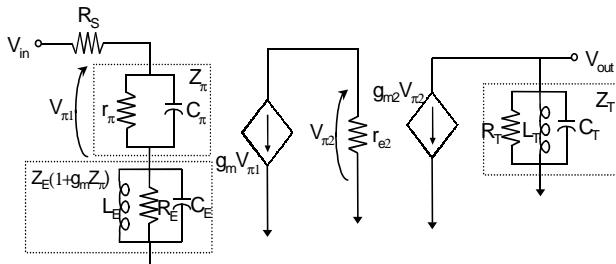


Fig. 2. Simple model of the LNA/filter for analysis.

The transfer function, $T(s)$, for this circuit can be derived using Fig. 2. With only minimal effort, it can be shown that:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m Z_\pi Z_T}{Z_E(1+g_m Z_\pi) + Z_\pi + R_s} \quad (1)$$

if the general case is now assumed where Z_T and Z_E are assumed to be parallel LCR tanks, and Z_π is assumed to be a resistor in parallel with a capacitor then the transfer function can be derived. After some manipulation the result is shown in (3).

Examining (3) stability must be ascertained. In order to do this the pole locations for (3) must be determined. This is a fifth order system with five poles. Two of the poles are from the tank at the collector of the cascode transistor and are safely in the left half plane.

$$T(s) = \frac{\frac{-g_m}{C_T} \left(s^3 + \frac{s^2}{C_E R_E} + \frac{s}{L_E C_E} \right)}{\left(s^2 + \frac{s}{C_T R_T} + \frac{1}{L_T C_T} \right) C_\pi R_s s^3 + \left(1 + \frac{C_\pi}{C_E} + \frac{R_s}{r_\pi} + \frac{C_\pi R_s}{C_E R_E} \right) s^2 + \left(\frac{1}{C_E R_E} + \frac{1}{r_\pi C_E} + \frac{g_m}{C_E} + \frac{R_s}{R_E C_E r_\pi} + \frac{C_\pi R_s}{L_E C_E} \right) s + \left(\frac{1}{L_E C_E} + \frac{R_s}{L_E C_E r_\pi} \right)} \quad (3)$$

The remaining poles are difficult to solve analytically so instead they are plotted with the assistance of Matlab in Fig. 3. It can be seen that even as R_E approaches infinity (as is the intention in this application) that the poles will remain in the left half plane. In fact, the circuit losses would have to be highly over compensated to drive them into the right half plane. From the plot it is easy to see that only if the losses in the emitter tank are overcompensated will the system become unstable. In practice however there should be some margin or the system may in fact start oscillating.

The zeros can also be determined from (3) as well. Letting R_E approach infinity and setting the numerator equal to zero, it is found that there are zeros at:

$$s_{1,2,3,4,5} = 0, \pm \frac{1}{L_E C_E}, \infty \quad (2)$$

Equation (2) shows clearly that the zeros of the system are placed at the frequency where the tank in the emitter resonates as expected.

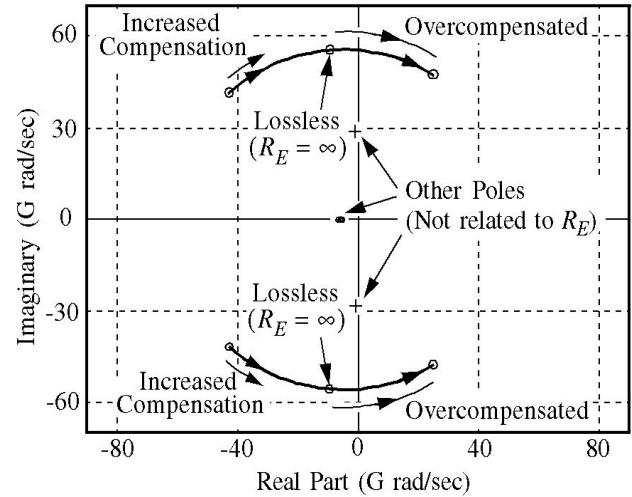


Fig. 3. Plot of the poles of the filter showing potential instability.

IV. INTERPRETATION OF FILTER STABILITY

The stability analysis fails to provide much design insight into the problem of making the filter stable. The

fundamental problem is non-trivial: how to stabilize an LC resonator specifically designed to have infinite Q? After all, an LC oscillator design begins with a resonator with infinite Q [6][7]. The mechanism for dampening the oscillation must come from either the source or load impedance. In previous work the cascode transistor provided dampening for the resonator. In this circuit the source impedance must damp the filter as shown in Fig. 4. If the source resistance is smaller than the tank resistance R_p then the tank can be safely tuned to provide infinite Q and still have ample dampening. However, if the tank resistance is smaller than the source resistance then even a small error in tuning the tank to infinite Q could result in oscillation.

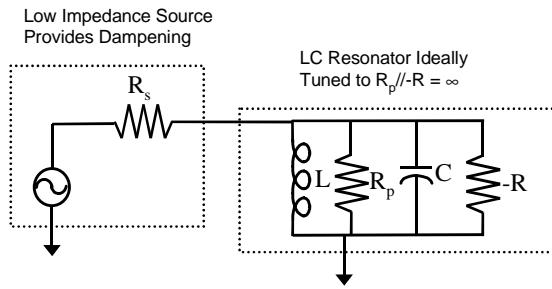


Fig. 4. Illustration of how the filter is damped without diminishing image rejection.

V. EXPERIMENTAL RESULTS

The test circuit was fabricated in a state of the art SiGe technology with 50GHz f_t . All components including the input inductor were fabricated on-chip. Care was taken in the layout of the circuit to ensure that signal tracks were kept as short as possible. Thick metal traces were used to provide a low inductance path to ground. The inductors were simulated and designed using Asitic [8]. As well, many tiedowns were used to try and isolate the inductors from the rest of the circuit. A photomicrograph of the circuit is shown in Fig. 5. The chip measured approximately 0.6mm by 0.5mm including pads.

The circuit was measured by wafer probing only. Using a network analyzer, the pass band gain was found to be 14 dB and the filter provided almost 56dB of attenuation at the image frequency. Thus the filter provides almost 70dB of image rejection. A plot of the filter response taken from the network analyzer is shown in Fig. 6. Overlaid on the same figure is a plot of the simulated response of the circuit with and without the notch circuitry for comparison.

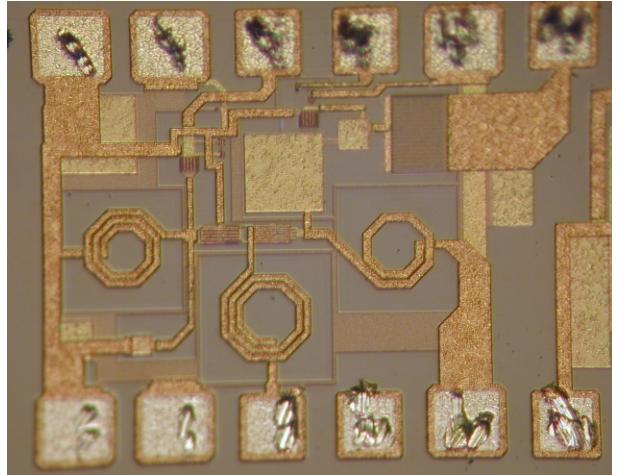


Fig. 5. Photomicrograph of the notch filter.

The pass band was centered at 4.6GHz and the notch can be varied from a frequency of about 6.3 to 6.8GHz. The plot of the notch frequency tuning characteristic is shown in Fig. 7. It can be seen from this plot that the tuning characteristic is quite linear. This is due to the excellent high Q varactors available in this process. The varactors employ a graded doping profile, which gives them a linear C-V curve. The result is a very linear tuning curve for the filter as well.

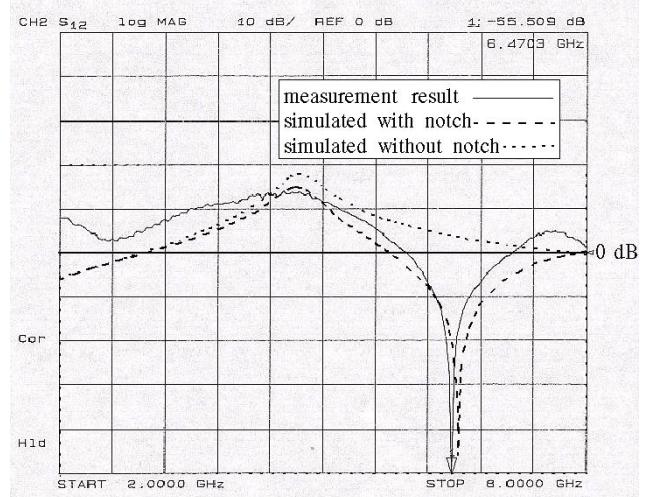


Fig. 6. Plot of the filter response showing 70dB of image rejection.

The notch was tuned by adjusting I_{sharp} to cancel all the losses in the circuit. It was found that in this case, a current of approximately 4mA was required to tune out the loss in the tank. This current varied slightly across the tuning range of the filter, nevertheless, with proper adjustment the image rejection was maintained across the entire tuning range.

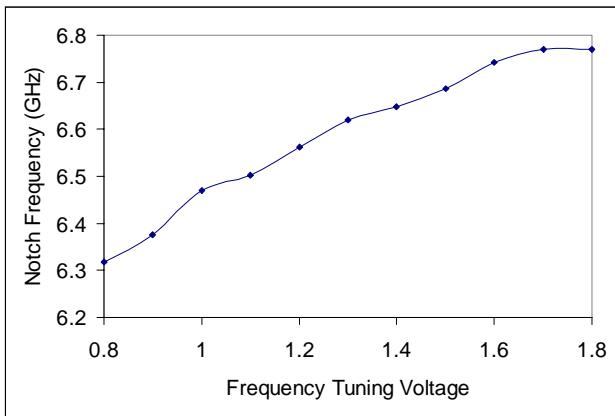


Fig. 7. Plot of the filter notch frequency response.

The input matching was done using on-chip inductors and was therefore poor compared to schemes using high-quality off-chip passive components. However, an S_{11} of -7.5dB was achieved showing that very little gain is lost in the circuit due to input mismatch.

The IIP3 was measured using a spectrum analyzer and applying two tones to the input in the pass band. It was found to be -6dBm for this circuit. A higher value could be achieved if more degeneration or current was used.

The noise figure was measured to be 4.2dB . The presence of the notch reduces the pass band gain of this circuit as can be seen in Fig. 6, which directly impacts the noise figure. Simulation showed the notch circuitry added about 1.5dB to the noise figure that could otherwise be achieved if the resonator was removed. Future experiments will move the inductor in the base off-chip in an attempt to improve the noise performance and matching of the circuit. Table I summarizes the measurements for this circuit.

Table I: Summary of Filter Performance

Parameter	Performance
S_{11} (series matching inductor on-chip)	-7.5dB
Current through Q1 (LNA)	6mA
Current through Q3 (resonator)	4mA
Supply Voltage	1.8Volts
IIP3	-6dBm
Gain (4.6GHz)	14dB
Image Rejection	70dB
Notch Tuning Range	$6.3\text{-}6.8\text{GHz}$
Noise Figure	4.2dB

VI. CONCLUSION

A 5GHz completely integrated notch filter has been realized in a SiGe process with 50GHz f_t . The filter uses no off-chip components and is suitable for wireless applications where a high degree of integration is desirable. The filter provides good gain, an excellent image rejection of almost 70dB and is tunable over a 500MHz bandwidth. Since the filter is implemented as part of the LNA little additional circuitry is required.

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